OPEN ACCESS
ISSN: 2249-6645

International
Journal
Of Modern Engineering Research (IJMER)

An Approach to Realize BIST Enabled UART Using VHDL

Parupalli Pravin Kumar[1], Ramkishore Reddy[2]
[1]*M.Tech Student ,CMR Engineering College, Telangana, India*
[2]*Assoc. Professor ,ECE Dept,CMREC,Telangana ,India*

ABSTRACT: *Testing of VLSI chips are becoming very much complex day by day due to increasing exponential advancement of nanotechnology. So both front-end and back-end engineers are trying to evolve a system with full testability keeping in mind the possibility of reduced product failures and missed market opportunities. BIST is a design technique that allows a system to test automatically itself with slightly larger system size. In this paper, the simulation result performance achieved by BIST enabled UART architecture through VHDL programming is enough to compensate the extra hardware needed in BIST architecture. This technique generate random test pattern automatically, so it can provide less test time compared to an externally applied test pattern and helps to achieve much more productivity at the end.*

Keywords: ***BIST, UART, VHDL, VLSI***

I. INTRODUCTION

The processing steps of VLSI chips are extremely complex, and costly inducing vendors to stress on more and more testability as a requirement tool to assure the reliability and the functionality of each of their designed circuits. BIST technique has become as a boon to them, which helps to test a system automatically. Universal Asynchronous Receive/Transmit (UART) has the objectives of firstly to satisfy specified testability requirements, and secondly to generate the lowest-cost with the highest performance implementation. UART has been an important input/output tool for decades and is still widely used. The additional BIST circuit that increases the hardware overhead increases design time and size of the chip, which may degrade the performance. This paper focuses on the design of a UART chip with embedded BIST architecture using simple LFSR with the help of VHDL language. The paper describes the problems of (VLSI) testing followed by the behavior of UART that includes both transmitter and receiver section using VHISC Hardware Description Language (VHDL). In this paper, The simulation result is compared with previous work and it has been seen that the result is promising and helps to reduce timing constraints and overall power dissipation.

i. HARDWARE SETUP

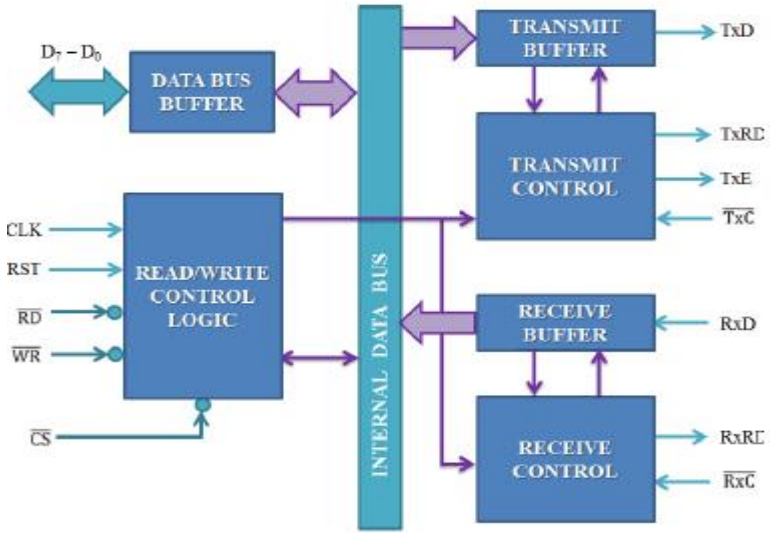

Figure 1: BIST ARCHITECTURE

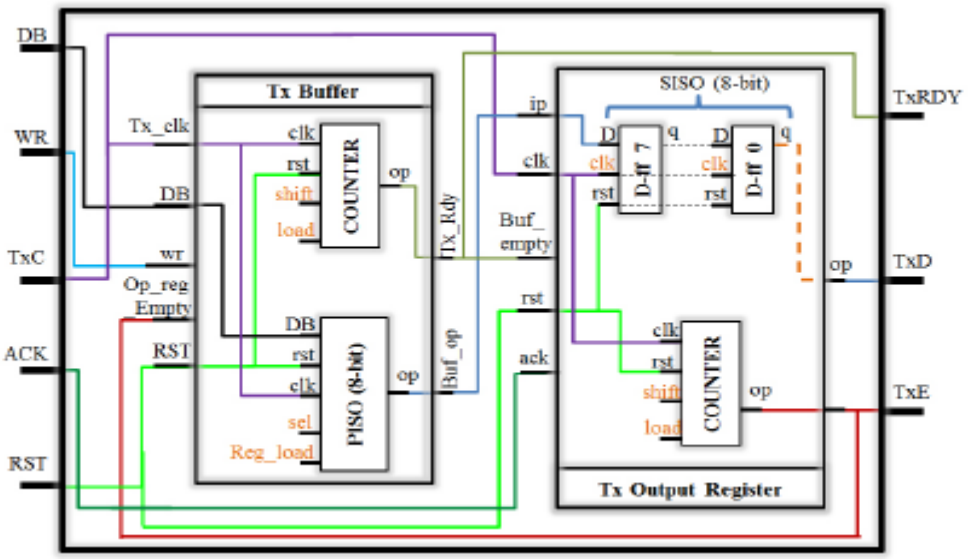

Figure 2: INTERNAL ARCHITECTURE OF UART TRANSMITTER

b. SOFTWARE USED

Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing.

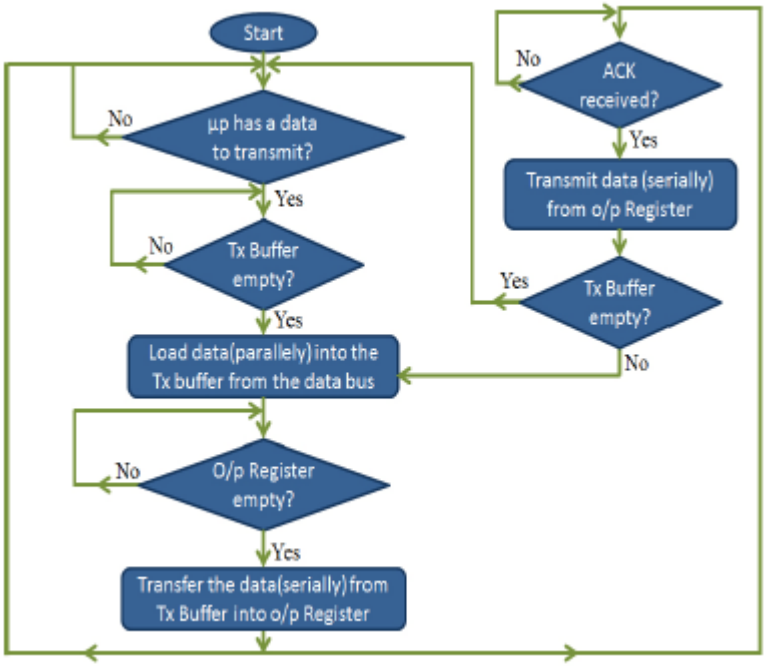

Figure 3: flow of entire process

II. CONCLUSION

This paper implements the VHDL language based coding for BIST technique on UART. UART transmitter and receiver sections are differently tested by BIST technique.

The transmitter is given a parallel 8 bit input and the serial output of the transmitter is checked with the respective ideal output stored in the ROM. The receiver is given a serial 8 bit input and the parallel output of the receiver is checked with the respective ideal output stored in the ROM. The checking part is done by comparator

section. It compares the receiver or transmitter output with the corresponding data stored in the ROM. Using memory BIST has various advantages such as no external test equipment, reduced development efforts, at-speed tests. However, there are many challenges associated with it such as silicon area overhead, extra pins and routing. In addition, the testability of the test hardware itself is another difficult task. An improvement can be made in the field of implementation of the Test Response Analyser (TRA). Rather than using ROM as TRA, Multiple Input Shift Register (MISR) can be used for the same purpose. All the simulation result presented in our paper shows that the BIST enabled UART is working well. Hardware test by FPGA Tool(Spartan2E) showed the same result as in the simulation result. The synthesis report that we got from the XILINX tool shows that it provides excellent result compared to the previous work.

REFERENCES

[1] *Mohd Yamani Idna Idris, Mashkuri Yaacob, Zaidi Razak*, "A VHDL Implementation Of UART Design with BIST capability"

[2] Dr. T.V.S.P. Gupta, Y. Kumari,M.Asok Kumar"UART realization with BIST architecture using VHDL" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 1, January -February 2013, pp.636-640

[3] M.S. Harvey,Generic UART Manual,Silicon Valley,December 1999

[4] P. J. Anderson , "The designer's guide to VHDL" , Morgan Kaufman ,2nd edition, 2002.

[5] Neil H.E. Weste, Kim Haase, David Harris , A. Banerjee , "CMOS VLSIDesign: A circuits and Systems Perspective", Pearson Education.

[6] K. Zarrineh, and S. J. Upadhyaya, "On programmable memory built-in

[7] self test architectures", Design, Automation and Test in Europe

[8] Conference and Exhibition 1999. Proceedings , 1999, pp. 708 -713.